AMRITA VISHWA VIDYAPEETHAM UNIVERSITY

श्रद्धावान् लभते ज्ञानम्

Established under Section 3 of the UGC Act 1956

AMRITA SCHOOL OF ENGINEERING, AMRITAPURI

MASTER OF TECHNOLOGY
IN
VLSI DESIGN
Grade Sheet: 2010-2012

Date of Birth: 23/05/1986

Name: Mr. Prajeesh R
RollNo: AM.EN.P2VLD10012

Code	Subject	Cr.	Gr.	Month & Year of Passing
First Semester				
MA607	Probability Theory and Linear Algebra	3.0	C+	Dec, 2010
VL601	CMOS Digital Integrated Circuits	4.0	C	Dec, 2010
VL602	Digital Hardware Modeling	3.0	C+	Dec, 2010
VL611	Solid State Devices Modeling and Simulation	3.0	A	Dec, 2010
VL612	Digital Design	4.0	C+	Dec, 2010
VL613	Digital Hardware Modeling Laboratory	1.0	B+	Dec, 2010
HU801	Cultural Education	0.0	P	Dec, 2010
Second Semester				
VL603	Digital Signal Processing and Processors	4.0	B	May, 2011
VL614	Analysis and Design of Analog and Mixed VLSI Circuits	4.0	C	May, 2011
VL615	Testing of VLSI Circuits	3.0	B	May, 2011
VL616	VLSI Design Laboratory	1.0	A+	May, 2011
VL701	Low Power VLSI Circuits	3.0	B+	May, 2011
VL708	VLSI Fabrication Technology	3.0	C+	May, 2011
VL710	RF IC Devices and Modelling	3.0	B+	May, 2011
Third Semester				
MA613	Orthogonal Functions, Optimization and Graph Theory	3.0	C	Dec, 2011
VL617	Computer Aided Design of VLSI Circuits	4.0	C+	Dec, 2011
VL798	Minor Project	4.0	B	Dec, 2011
RW703	Adaptive Digital Signal Processing using FPGA	4.0	C+	Dec, 2011
VL721	Advanced Analog Design	3.0	C	Dec, 2011
Fourth Semester				
VL799	Dissertation	10.0	C	Jul, 2012

Summary: Grade Point Average (GPA) on a 10 Point Scale

Semester	1	2	3	4
Semester GPA	7.39	7.86	6.89	6.00

The cumulative grade point average of the candidate (CGPA) is 7.19

Deputy Controller of Examinations
Amritapuri Campus

Date Issued On: August 6 , 2012

Controller of Examinations

Register No : 41203803/41203407/04411012

UNIVERSITY OF KERALA

कर्मणि व्यज्यते प्रज्ञा

കേരള സർവകലാശാല

FACULTY OF ENGINEERING AND TECHNOLOGY

The Senate of the University of Kerala hereby makes known that **Prajeesh, R.** *has been admitted to the Degree of Bachelor of Technology under* **Electronics and Communication Engineering** *Branch, he having been certified by duly appointed examiners to be qualified to receive the same and having been by them placed in the* **First Class** *at the examination held in* **July 2008** .

Given under the seal of the University

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University Buildings
Thiruvananthapuram **January 23, 2009**

Vice Chancellor