



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
HYDERABAD - 500 085, ANDHRA PRADESH, INDIA



CONSOLIDATED MARKS MEMO / CREDIT SHEET

Master of Technology- DIGITAL ELECTRONICS & COMMUNICATION SYSTEMS

CMM. No. : **C 0119219**

Serial No. : 20175003153

Name : PANDITI SUNEEL KUMAR

Hall Ticket No. : 09P81D3812

Year of Admission : 2009-2010

Name of the College : P8-JIET, CHINTHAPALLIGUDA

Month & Year of Final Exam : January, 2012

Class Awarded : **FIRST CLASS WITH DISTINCTION**

S.No	SUBJECT TITLE	INT MARKS	EXT MARKS	Total Marks	Pass(P)/ Fail(F)
	Maximum Marks in Lab	40	60	100	

I SEMESTER

1	DIGITAL SYSTEM DESIGN	39	26	65	P
2	EMBEDDED REAL TIME OPERATING SYSTEMS	40	24	64	P
3	SIGNAL PROCESSING LAB	40	59	99	P
4	SEMINAR	49	-	49	P
5	ADVANCED DIGITAL SIGNAL PROCESSING	39	44	83	P
6	VLSI TECHNOLOGY AND DESIGN	39	24	63	P
7	ADVANCED DATA COMMUNICATIONS	39	28	67	P
8	MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN	39	37	76	P

II SEMESTER

1	IMAGE & VIDEO PROCESSING	39	45	84	P
2	DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES	39	37	76	P
3	ADVANCED COMMUNICATIONS LAB	40	56	96	P
4	SEMINAR - II	46	-	46	P
5	CODING THEORY AND TECHNIQUES	39	24	63	P
6	OPTICAL COMMUNICATIONS TECHNOLOGY	39	27	66	P
7	WIRELESS COMMUNICATIONS & NETWORKS	39	28	67	P
8	LOW POWER VLSI DESIGN	39	26	65	P

III SEMESTER

1	COMPREHENSIVE VIVA - VOCE	-	89	89	P
(Comprehensive VIVA External= 100)					

IV SEMESTER

1	PROJECT WORK*	-	B	-	P
(* A - Excellent, B - Good, C - Satisfactory, D - Un Satisfactory)					

Aggregate Marks Secured : **1218 OUT OF 1600 (76.12%)**

Date of Issue : **May 16, 2012**
(see overleaf for Rules concerned to award of class)



(*Courses registered but not counted for calculation of aggregate)

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CONTROLLER OF EXAMINATIONS