Impact of high k materials in Low power techniques

Low Power VLSI Chips is important issue due to high device density, high operating frequency, proliferation of portable consumer electronics, concerns on environments and energy sources. Increasing power consumption and degrading device performance are observed when SiO2 is used as a gate insulator in FET. Therefore, the high-κ dielectric materials (Al2O3, La2O3, and ZrO2) are considered as promising solutions to improve the gate control on the channel region and the electrical performance . The region between the source and the drain of the considered low power device is to be covered by implementing high-κ gate dielectric materials which allow further miniaturization of electronic components , higher value of gate dielectric constant can increase the drain current and improve the leakage current & leads to decrease in power consumption. Drain induced barrier lowering is reduced with the increase in gate dielectric constant. High-κ materials are more suitable than the well-known SiO2 due to the smaller thickness required which decreases the threshold voltage and improves the leakage characteristics of the device. Here implementation of high k materials is to be considered. The influence of the gate dielectrics on threshold voltage roll-off, sub threshold slope, trans conductance, drain induced barrier lowering, leakage current, on-current, and on/off current ratio is to be investigated in the future work.

K.Kalai Selvi AP/ECE
Government College of Engineering
Tirunelveli