

# **DESIGN OF A NOVEL ENCODING MECHANISM USING SOLS TECHNIQUE FOR DEDICATED SHORT RANGE COMMUNICATION**

## **ABSTRACT**

Due to the popularity of portable electronic products, low power system has attracted more attention in recent years. Dynamic power consumption remains to be the biggest contributor to the total power consumption of a hardware design. One of the major sources for dynamic power consumption is the system's clock signal, which is responsible for thirty to seventy percentage of the total dynamic power consumption. Several techniques to reduce the dynamic power were developed, among which clock gating is predominant. To reduce unwanted switching of clock signals, clock gating technique is used. Various clock gating techniques are available, of which Look-Ahead Clock Gating (LACG) plays a dominant role to reduce power consumption.

This project presents a novel Linear Feedback Shift Register (LFSR) with LACG technique for power reduction in sequential circuits. LACG computes the clock enabling signals of each flip-flop one cycle ahead of time, based on the present cycle data of those flip-flops on which it depends. Simulation results using CADENCE shows that, the LFSR with the LACG technique exhibit resourceful power reduction compared to the non-gated clock LFSR and data-driven clock gating LFSR.

To improve the power reduction in the LFSR with LACG technique, the concept of flip-flop grouping is performed in this project which is based on the toggling probability. The novel grouped LFSR with LACG technique can be applied for various applications like Pseudo Random Number Generators (PRNGs), Built In Self Test (BIST), Signature analysis and Spread spectrum communication systems for power reduction. In this project, the proposed technique is applied to the application circuit called BIST for reducing the dynamic power consumption.

