Proposed Area and Topic of research

Candidate Name : PRAJEESH R

Area of Research : VLSI

Proposed title: Short channel effects in Negative Capacitance FinFETs

Objectives: The main objective is to analyze the short channel effects in metal-ferroelectric-insulator-semiconductor (MFIS)-type negative capacitance FinFET and a comparison with negative capacitance MOSFET

Research problem:

The multigate FETs accompanied by a high-k/metal gate-stack have played a key role in controlling the short channel effects (SCEs) and the leakage current.

The negative capacitance (NC) effect causes opposite trends in short channel effects like threshold voltage roll-up and negative DIBL. The NCFET enables effectively lowering of the power supply voltage of conventional metal oxide semiconductor field effect transistor (MOSFET).

The negative capacitance effect leads to enhancement of drain current for small voltage operation.

Research methodology:

In this research I would like to analyze the short channel effects in metal-ferroelectric-insulator-semiconductor (MFIS)-type negative capacitance FinFET (NC-FinFET) using 3-D technology computer-aided design (TCAD) simulations.

References:

1. A. D. Gaidhane, G. Pahwa, A. Verma and Y. S. Chauhan, "Gate-Induced Drain Leakage in Negative Capacitance FinFETs," in *IEEE Transactions on Electron Devices*, vol. 67, no. 3, pp. 802-809, March 2020, doi: 10.1109/TED.2020.2967463.

2. H. Ota et al., “Perspective of negative capacitance FinFETs investigated by transient TCAD simulation,” in IEDM Tech. Dig., Dec. 2017, pp. 15.2.1–15.2.4, doi: 10.1109/IEDM.2017.8268394.

3. W. You, C. Tsai and P. Su, "Short-Channel Effects in 2D Negative-Capacitance Field-Effect Transistors," in IEEE Transactions on Electron Devices, vol. 65, no. 4, pp. 1604-1610, April 2018, doi: 10.1109/TED.2018.2805716.