RESEARCH PROPOSAL

Domino CMOS circuits are significantly used in high performance very large scale integrated system. Designing a low power with high speed performance VLSI circuit is one of the challenging aspects. Full adder is one of the basic blocks for many circuits for multiplication, division and exponentiation operation. To increase the performance of VLSI circuits and integrate more functionality into every chip, the size of the transistor is continually shrinking day by day which results in the complexity of chips and power consumption.

Domino logic style is generally used for designing a high performance circuit, rather than a static logic style. For arithmetic operations full adder acts as a basic element for parity checker, comparator and multiplier, hence it receives a lot of attention by the researchers.

In this research, I am focusing to optimize the performance parameter of CMOS based, full adder in terms of power and delay. Generally the power and the delay are the two factors which can’t be reduced both at a same time, but these parameters can be optimized.