APPROXIMATE AND POWER EFFICIENT TRUNCATED BOOTH MULTIPLIERS USING APPROXIMATE CARRY BASED ERROR COMPENSATION

ABSTRACT

Approximate computing is a promising technique to elevate the performance of digital circuits at the cost of reduced accuracy in numerous error-resilient applications. Multipliers play a key role in many of these applications. A truncation-based Booth multiplier with a compensation circuit generated by selective modifications in k-map to circumvent the carry appearing from truncated part is proposed in this brief. By judicious mapping, hardware pruning and output error reduction is achieved simultaneously. In the quest of power and accuracy trade-off, Truncated and Approximate Carry based Booth Multipliers (TACBM) are proposed with a range of designs based of truncation factor w. When compared with state-of-the-art multipliers, TACBM outperforms in terms of accuracy and Area Power Savings. TACBM(W=10) provides 23% reduction in Area Power product compared to Booth multiplier. The multipliers are evaluated using image blending and Multilayer perception (MLP) neural network and a high value of accuracy (95.63%) for MLP is achieved.