DESIGN OF VARIOUS FAULT TOLERANT REVERSIBLE ADDERS USING HYBRID MPG- F2G FOR POWER AND AREA OPTIMIZATION

Adder circuit is central to most digital circuits that slaves a significant port in the design of particular integrated circuits. Power dissipation and delay and area are the momentous parameter of the circuits. This research focus on improving the performance of reversible adders by incorporating gating techniques like clock gating and power gating.A MPG (Modified peres gate) hybrid with F2G(Feynman Double Gate) is proposed to improve the power efficiency and fault tolerance,also to minimize the parameters such as delay and fabrication area.MPG is designed in such way that 3T EXOR and 2T AND gate which minimize the area and power consumption also it preserves parity under reversible gates.F2G consists of Feyman Gate with an extra input and one more output which is used in copying the signal that avoids fanout problems in reversiblelogic circuit design.thus the proposed Reversible Logic adder using Hybrid MPG-F2G is expected to improve the power efficiency as well as to minimize the fabrication area.The Schematic is to be designed in DSCH2 and layout in Microwind EDA Tool.