STATEMENT OF RESEARCH PROPOSAL

1 TITLE:

Advanced Dielectric and Interface Strategies for Next-Generation HEMTs: TiN/High-k Gate Stack on InP-Capped InAlAs Channels

2. AREA OF RESEARCH AND DOMAIN OF RESEARCH:

VLSI Design

3. OBJECTIVE OF THE PROPOSAL:

This research aims to develop and optimize advanced dielectric and interface engineering strategies for next-generation High Electron Mobility Transistors (HEMTs) utilizing a TiN/high-k gate stack on InP-capped InAlAs channels. The focus is on enhancing device performance in terms of frequency response, leakage control, and threshold voltage stability. By investigating the impact of the TiN/high-k integration on interface quality, carrier transport, and dielectric reliability, this work seeks to overcome scaling limitations and enable high-performance, low-power HEMT designs using TCAD. Comprehensive electrical and material characterization will support the development of scalable, CMOS-compatible solutions for future high-speed and high-frequency electronic applications.

4. SHORT DESCRIPTION:

PROBLEM TO BE RESOLVED:

- To reduce gate leakage and improve dielectric reliability by optimizing the integration of the TiN/high-k gate stack in InP-capped InAlAs channel HEMTs.
- To minimize interface trap density at the high-k/InAlAs interface to enhance carrier mobility, subthreshold swing, and overall device switching performance.
- To improve threshold voltage stability under prolonged bias conditions by addressing charge trapping mechanisms within the gate dielectric and at critical interfaces.

AVAILABLE SOLUTIONS:

Optimizing interface engineering, using surface passivation, and tailoring TiN/high-k deposition techniques can reduce leakage, improve stability, and enhance mobility in InP/InAlAs HEMTs.

5 EXPECTED RESULTS:

- Significant reduction in gate leakage and improved threshold voltage stability due to optimized TiN/high-k gate stack integration, leading to enhanced device reliability and low-power operation.
- Improved carrier mobility and higher RF performance metrics (fT, fmax), enabled by reduced interface trap density at the high-k/InAlAs interface and better electrostatic control from the InP cap layer.

6 REFERENCES:

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[5] Chou, Y.-C., & Lee, C.-T. (2005). Degradation mechanism and reliability improvement of InGaAs/InAlAs/InP HEMTs using new gate metal electrode technology. In *IEEE International Conference on Indium Phosphide & Related Materials* (p. 223). □cite□turn0search13□□